Here's a basic Verilog HDL source code for modeling a CMOS inverter circuit. In CMOS technology, an inverter is a fundamental building block that outputs the opposite logic level of its input. The CMOS inverter consists of a PMOS and an NMOS transistor connected in series.

\*Verilog Code:\*

verilog

// CMOS Inverter Module

module cmos\_inverter (

input wire A, // Input signal

output wire Y // Output signal

);

// Internal wire for PMOS and NMOS gates

wire nA;

// Logic for NMOS and PMOS transistors

assign nA = ~A; // NMOS transistor pulls the output low when input is high

assign Y = nA; // PMOS transistor pulls the output high when input is low

endmodule

\*Description of Project:\*

1. \*Project Overview:\*

The project involves creating a CMOS inverter circuit using Verilog HDL to demonstrate the basic principles of CMOS technology, which is fundamental for digital logic operations.

2. \*Problem Statement:\*

Implementing a CMOS inverter circuit in Verilog HDL to understand the transformation of logic levels and the operation of CMOS transistors in digital circuits.

3. \*Tools and Applications Used:\*

- \*Verilog HDL\* for hardware description.

- \*Simulation Tools\* like ModelSim or XSIM for verifying the design.

4. \*Detailed Description of Sub-Modules:\*

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- \*Input:\* Signal A is fed into the inverter.

- \*Inversion Process:\* The internal wire nA inverts the input signal.

- \*Output:\* The final output Y reflects the inverted logic level of the input signal A.

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